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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/714,258	11/14/2003	Kevin D. Safford	200206544-1	3628

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EXAMINER	
CHU, GABRIEL L	
ART UNIT	**PAPER NUMBER**
2114	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/20/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/714,258	SAFFORD ET AL.	
	Examiner	Art Unit	
	Gabriel L. Chu	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6 and 8-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6 8-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-4, 8-11 rejected under 35 U.S.C. 102(b) as being anticipated by US 20020133745 to Okin.

3. Referring to claim 1, 8, Okin discloses a processor that includes a mechanism for detecting soft errors comprising:

a) instruction fetch unit for fetching an instruction; b) an instruction decoder for decoding the instruction (From paragraph 1, "The microprocessor (22) is connected to external cache memory (32) and a main memory (34) that both hold data and program instructions to be executed by the microprocessor (22). Internally, the execution of program instructions is carried out by the CPU (24).");

c) duplication hardware for duplicating the instruction; d) a first execution unit for executing the instruction in a first execution cycle; e) the first execution unit executing the duplicated instruction in a second execution cycle; f) comparison hardware for comparing the results of the first execution cycle and the results of the second execution cycle; and g) a commit unit for committing one of the results when the results

are the same; and h) an exception unit for generating an exception (raising a fault) when the results are not the same (From paragraph 27, 28, "FIG. 3 is a flow chart showing an exemplary self-checking operation. Generally, the process involves starting in series both Thread A and Thread B at the same program location. The starts are separated temporally by the time between the beginning of execution and an I/O request generating event. For example, if Thread A begins execution, at some point in time, Thread A issues a read or write request external to the processor. At that point, Thread A is blocked and Thread B begins processing the same instructions that Thread A just processed. At some point in time thereafter, Thread B issues the same I/O request, if all the internal circuitry is performing properly. That is, there has been no effects on the processor by cosmic event, internal noise, or other defect. Once both threads have confirmed the same I/O request, the I/O request is issued externally. Thus, any I/O request issued is free of transient events and the decision areas of the processor have been verified to have acted consistently. Referring directly to the exemplary flow shown in FIG. 3, Thread A processes the program (step 200) until an I/O request is generated (step 202). Upon generation of the I/O request, Thread A is suspended (step 204) and Thread B processes the same section of the program (Step 206). When Thread B reaches the point at which Thread A generated an I/O request, if all processor components are properly functioning, Thread B will generate an identical I/O request (step 208). Upon generation of the I/O request by Thread B (step 208), the self-checking component compares the I/O requests generated by Thread A and Thread B (step 210). If the I/O requests are the same (step 210), the I/O request has

been verified as error-free and can be issued externally (step 212). On the other hand, if the I/O requests do not match (step 210), it is clear that some intervening event caused an inconsistency. Thus, processing is suspended (step 214) and remedial action is taken. Dependent on circumstance, the remedial action may be reprocessing the program, returning an error, or the like.").

4. Referring to claim 2, 9, Okin discloses the step of executing the instruction in a first execution cycle includes the step of storing the results of the first execution cycle (From paragraph 28, "Referring directly to the exemplary flow shown in FIG. 3, Thread A processes the program (step 200) until an I/O request is generated (step 202). Upon generation of the I/O request, Thread A is suspended (step 204) and Thread B processes the same section of the program (Step 206).").

5. Referring to claim 3, 10, Okin discloses the step of executing the instruction in the first execution cycle includes issuing the decoded instruction to a first execution unit; and wherein the step of executing the instruction in the second execution cycle includes issuing the decoded instruction to the first execution unit (From paragraph 27, "FIG. 3 is a flow chart showing an exemplary self-checking operation. Generally, the process involves starting in series both Thread A and Thread B at the same program location. The starts are separated temporally by the time between the beginning of execution and an I/O request generating event. For example, if Thread A begins execution, at some point in time, Thread A issues a read or write request external to the processor. At that point, Thread A is blocked and Thread B begins processing the same instructions that

Thread A just processed. At some point in time thereafter, Thread B issues the same I/O request, if all the internal circuitry is performing properly.").

6. Referring to claim 4, 11, Okin discloses the first execution unit is one of floating point unit, an integer unit, a arithmetic logic unit (ALU), a multimedia unit, and a branch unit (From paragraph 1, "Computer processors comprise arithmetic, logic, and control circuitry that interpret and execute instructions from a computer program. ").

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 5, 6, 12, 13 rejected under 35 U.S.C. 103(a) as being unpatentable over US 20020133745 to Okin as applied to claim 1, 8 above, in further view of US 6640313 to Quach.

9. Referring to claim 5, 12, although Okin does not specifically disclose a control register that includes a bit for enabling the duplication hardware and comparison hardware, selectively enabling lockstep is known in the art. An example of this is shown by Quach, from line 60 of column 5, "For the disclosed embodiment of processor 100, PSR 180 includes a mode status bit (MSB) 184, which indicates whether processor 100 is in HR mode or HP mode. For purposes of illustration, a value of one in MSB 184 indicates that processor 100 is in HR mode, and a value of zero indicates that processor

100 is in HP mode." Further, from line 18 of column 4, "In HR mode, the issue module provides identical instructions to each of execution clusters and compares the results generated by each cluster to identify errors. In HP mode, the issue module provides instructions to the execution clusters independently, significantly increasing the processor's instruction throughput. The processor may be switched between HP and HR modes through explicit mode switch instructions or in response to certain mode switch events, e.g. issue of instructions from a memory region that is designated as UC." A person of ordinary skill in the art at the time of the invention would have been motivated to switch between such HP and HR modes because, as shown by Quach, "In HR mode, the issue module provides identical instructions to each of execution clusters and compares the results generated by each cluster to identify errors. In HP mode, the issue module provides instructions to the execution clusters independently, significantly increasing the processor's instruction throughput."

10. Referring to claim 6, 13, Okin in view of Quach discloses the bit is set by one of user-programmed firmware and an operating system (From line 17 of column 8 of Quach, "The disclosed embodiment of processor 100 may switch between HR and HP modes in response to mode switch instructions (or instruction bundles) or on the occurrence of certain conditions, e.g. issue of an instruction from a region of memory designated as UC. In the following discussion, S_HR represents one or more instructions that switch processor 100 from HP to HR mode ("HP-to-HR mode switch"), and S_HP represents one or more instructions that switch processor 100 from HR to HP mode ("HR-to-HP mode switch"). Mode switch instructions may be scheduled through

an application, e.g. by a linker, following compilation, by a firmware routine, by the operating system (OS) code or some combination of these codes.").

11. Claims 14-19 rejected under 35 U.S.C. 103(a) as being unpatentable over US 20020133745 to Okin in view of US 6640313 to Quach.

12. Referring to claim 14, 17, Okin discloses a method an error detection mechanism that employs alternating threads (See above, abstract.).

Although Okin does not specifically disclose selectively enabling by a) maintaining a control register that includes an error detection enable bit; b) setting the error detection enable bit to enable the error detection mechanism; and c) clearing the error detection enable bit to disable the error detection mechanism, this is known in the art. An example of this is shown by Quach, from line 60 of column 5, "For the disclosed embodiment of processor 100, PSR 180 includes a mode status bit (MSB) 184, which indicates whether processor 100 is in HR mode or HP mode. For purposes of illustration, a value of one in MSB 184 indicates that processor 100 is in HR mode, and a value of zero indicates that processor 100 is in HP mode." Further, from line 18 of column 4, "In HR mode, the issue module provides identical instructions to each of execution clusters and compares the results generated by each cluster to identify errors. In HP mode, the issue module provides instructions to the execution clusters independently, significantly increasing the processor's instruction throughput. The processor may be switched between HP and HR modes through explicit mode switch instructions or in response to certain mode switch events, e.g. issue of instructions from a memory region that is designated as UC." A person of ordinary skill in the art at the

time of the invention would have been motivated to switch between such HP and HR modes because, as shown by Quach, "In HR mode, the issue module provides identical instructions to each of execution clusters and compares the results generated by each cluster to identify errors. In HP mode, the issue module provides instructions to the execution clusters independently, significantly increasing the processor's instruction throughput."

13. Referring to claim 15, 18, Okin in view of Quach discloses the step of setting the error detection enable bit to enable the error detection mechanism includes one of a user-programmed firmware setting the error detection enable bit to enable the error detection mechanism; an operating system setting the error detection enable bit to enable the error detection mechanism; and an application setting the error detection enable bit to enable the error detection mechanism; and wherein the step of clearing the error detection enable bit to disable the error detection mechanism includes one of a user-programmed firmware clearing the error detection enable bit to enable the error detection mechanism; an operating system setting clearing the error detection enable bit to enable the error detection mechanism; and an application clearing the error detection enable bit to enable the error detection mechanism (From line 17 of column 8 of Quach, "The disclosed embodiment of processor 100 may switch between HR and HP modes in response to mode switch instructions (or instruction bundles) or on the occurrence of certain conditions, e.g. issue of an instruction from a region of memory designated as UC. In the following discussion, S_HR represents one or more instructions that switch processor 100 from HP to HR mode ("HP-to-HR mode switch"),

and S_HP represents one or more instructions that switch processor 100 from HR to HP mode ("HR-to-HP mode switch"). Mode switch instructions may be scheduled through an application, e.g. by a linker, following compilation, by a firmware routine, by the operating system (OS) code or some combination of these codes.").

14. Referring to claim 16, 19, Okin in view of Quach discloses the error detection mechanism is enabled for a portion of critical code that includes a first instruction and a last instruction; wherein the step of setting the error detection enable bit to enable the error detection mechanism includes the step of setting the error detection enable bit to enable the error detection mechanism prior to the execution of the first instruction of the critical portion of code; and wherein clearing the error detection enable bit to disable the error detection mechanism includes clearing the error detection enable bit to disable the error detection mechanism after the execution of the last instruction of the critical portion of code (From line 17 of column 8 of Quach, "The disclosed embodiment of processor 100 may switch between HR and HP modes in response to mode switch instructions (or instruction bundles) or on the occurrence of certain conditions, e.g. issue of an instruction from a region of memory designated as UC. In the following discussion, S_HR represents one or more instructions that switch processor 100 from HP to HR mode ("HP-to-HR mode switch"), and S_HP represents one or more instructions that switch processor 100 from HR to HP mode ("HR-to-HP mode switch"). Mode switch instructions may be scheduled through an application, e.g. by a linker, following compilation, by a firmware routine, by the operating system (OS) code or some combination of these codes.").

Conclusion

15. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See notice of references cited.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gabriel L. Chu whose telephone number is (571) 272-3656. The examiner can normally be reached on weekdays between 8:30 AM and 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Scott Baderman can be reached on (571) 272-3644. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Gabriel L. Chu
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gc